REMARKS

Reconsideration and allowance of the subject application are respectfully requested.

The typographical error in claim 15 has been corrected. Withdrawal of the objection to claim 15 is requested.

Claims 11 and 24 stand rejected under 35 U.S.C. §112, second paragraph. Claims 11 and 24 have been amended to delete the phrase "both behaviors" and the behaviors (i) and (ii) specifically recited in claim 8 upon which claim 11 depends are specifically recited. Claim 24 has been amended to depend from claim 21 and to include the behaviors (i) and (ii) specified in claim 21. Withdrawal of the objection under 35 U.S.C. §112, second paragraph is respectfully requested.

Applicants note with appreciation the Examiner's withdrawal of the earlier prior art rejection based on the description of the prior art section on pages 2 and 3 of the originally filed specification in view of Westcott. However, the Examiner makes a new ground of rejection under 35 U.S.C. §103. Specifically, claims 1-4, 7, 12-17, and 20 stand rejected under 35 U.S.C. §103 as being unpatentable over the description of the prior art, (referred as to "DPA"), in view of newly-applied Dale. This rejection is respectfully traversed.

The Examiner contends that the DPA discloses all features in the independent claim except for "generating a data place holder or insertion of late data into a data stream." The Examiner asserts that Dale remedies these deficiencies. Applicants disagree.

Generating a trace data stream representing the step-by-step activity of a processor is troublesome when completing one instruction is not required before starting execution of a subsequent instruction. Consider a data "miss" where a data value is not present in cache memory and must be retrieved from the main memory, thereby incurring a delay of possibly

several processing cycles. Although it is known for a processor to continue generating program instructions while awaiting data from a previous load miss, it is not known how to provide a meaningful trace data stream that enables correlation of the data being recovered later from memory with the earlier executed instructions. The inventors solved this problem by (1) providing a data place holder in the trace data stream in response to a data miss, and (2) inserting an identifier for the data value at a later point in the trace data stream when a successful access to the missing data value has been made. The place holder and identifier can then be subsequently matched together.

Dale describes an apparatus for instruction execution tracing with out-of-order, speculative processors. As explained at column 5, beginning at line 9, instructions and data are loaded into their respective caches 406 and 404, and address and content information for those instructions and data are captured by a trace buffer 490. This buffered information is then sent to and stored in a trace storage 495, and that stored data is used to construct a "snap shot" of the caches 406 and 404. Contrary to what is recited in the independent claims, Dale stores instruction address information for all fetched instructions and data in sequential order in the trace storage device 495. See column 5, lines 35-38. Dale later reconstructs the entire sequence of fetched instructions from the sequentially stored information in the trace storage device 495. See, for example, column 5, lines 38-44:

> In this way, a real time sequential listing of all instructions fetched by the fetch unit 420 may be obtained. This sequential listing may be used to reconstruct the instruction stream of an executed program, i.e. the particular instruction sequence or code created by the programmer of the program.

In contrast, the independent claim 1 recites that the trace circuit is "responsive to said data miss to generate a data place holder within said stream of trace data at a position where data

identifying said data value would have been placed if said data misses had not occurred." Because only data misses generate data place holders, much less trace data needs to be correlated than in Dale's approach where information for every fetched instruction is stored in the trace storage device 495 and used to reconstruct each instruction of an executed program.

The Examiner refers to column 2, lines 16-19 in Dale as allegedly teaching a tracing circuit responsive to a data miss to generate a data place holder within a stream of trace data. Applicants disagree. This text—read in context—teaches that an identifier is stored along with address information for every scheduled instruction. As explained at column 6, lines 42 and on, as each of the instructions is sequenced by the sequencing unit 450, a unique identifier, associated with each instruction, is ultimately stored in the trace storage device 495 along with the instruction address. In other words, the unique identifier is created, not in response to a data miss, but instead simply as a result of instructions being sequenced for execution. Dale's identifiers are used to track execution of each instruction to create a sequential execution list later used to reconstruct the instruction stream.

The Examiner also contends that column 2, lines 7-10 of Dale discloses the feature of claim 1 that when access to the data value resulted in the data misses does actually occur, a late data value is inserted with an identifier at a later point in the trace data stream. Applicants again disagree. This passage in Dale discloses that updated cache information is stored in the trace storage device 495 when a cache load is required to obtain non-cached data or instructions. As explained at column 5, lines 16-21, address information is stored in the data structure of the traced storage device 495 in response to a cache load. Dale requires an instruction stream reconstruction device 750 to correlate a stored cache model 740 with instruction stream event information stored in memory 730 to reconstruct the entire instruction stream. Dale's approach is

quite different from what is recited in the independent claims in which the late accessed data value is simply inserted into the trace data stream of the identifier when that data value actually becomes available at a subsequent point in time after the initial access request.

Lacking features recited in the independent claims and advantages associated with those features as explained above. The rejections based on DPA and Dale should be withdrawn. The application is in condition for allowance. An early notice to that effect is earnestly solicited.

Respectfully submitted,

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